POINT 1902 LOMA
NAZARENE UNIVERSITY

Department of Physics and Engineering

EGR3093 Digital Electronics

2 Units

Spring 2024

TR | 10:00 - 10:50 AM ; T | 1:30 PM - 4:20 PM

Meeting location Rohr Science Hall (RS) 365

Final Exam: 04/30 10:30 AM - 12:00 PM

Instructor title and name:	Dr. José Manjarrés
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PLNU Mission

To Teach ~ To Shape ~ To Send

Point Loma Nazarene University exists to provide higher education in a vital Christian community where minds are engaged and challenged, character is modeled and formed, and service is an expression of faith. Being of Wesleyan heritage, we strive to be a learning community where grace is foundational, truth is pursued, and holiness is a way of life.

Department Mission

The Physics and Engineering Department at PLNU provides strong programs of study in the fields of Physics and Engineering. Our students are well prepared for graduate studies and careers in scientific and engineering fields. We emphasize a collaborative learning environment which allows students to thrive academically, build personal confidence, and develop interpersonal skills. We provide a Christian environment for students to learn values and judgment, and pursue integration of modern scientific knowledge and Christian faith.

Course Description

Boolean algebra, logic gates, combinational logic circuits, state minimization, flip/flops, sequential circuits, asynchronous and synchronous counters. The course emphasizes design aspects using electronic design software.

Prerequisite(s): EGR 2024 with a grade of C- or higher.
Corequisite(s): EGR 3093L

Program and Course Learning Outcomes

Student Outcomes:

- Comprehend and apply various number systems such as binary, decimal, and hexadecimal, and effectively perform conversions between these systems.
- Develop a strong understanding of Boolean logic, including constants and variables, and effectively use truth tables for analyzing and designing logic circuits.
- Describe logic circuits algebraically and evaluate their outputs, utilizing Boolean theorems and algebraic simplifications.
- Demonstrate the ability to design and analyze combinational logic circuits, including the application of the Karnaugh Map method.
- Understand and design sequential logic circuits, including flip-flops and their applications in frequency division and counting while considering timing constraints and implications.
- Implement and analyze digital arithmetic circuits.
- Design and interpret state machines and apply project management skills in creating practical digital system projects.

Program Outcomes:

- An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics. (LO1)
- An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors. (LO2)

- An ability to communicate effectively with a range of audiences. (LO3)

Required Texts and Recommended Study Resources

- Widmer, N. Moss, G. Tocci, R. Digital Systems: Principles and Applications, 12th ed. Pearson, 2017. ISBN 9780134220130.

Course Credit Hour Information

In the interest of providing sufficient time to accomplish the stated Course Learning Outcomes, this class meets the PLNU credit hour policy for a 3-unit class delivered over 14 weeks. It is anticipated that students will spend a minimum of 37.5 participation hours per credit hour on their coursework. For this course, students will spend an estimated 75 total hours meeting the course learning outcomes.

Assessment and Grading

The table below outlines the assessment criteria for this course.

Activity	Points Per Activity	Quantity	Total Points
Knowledge Checks	20	5	100
Entry Tickets	10	7	70
Project Presentations	50	4	200
Class Participation	20	23	460
			830

Grades will be based on the following:

Sample Standard Grade Scale Based on Percentages

A	B	C	D	F
A 93-100	B+ 87-89	C+ 77-79	D+ 67-69	F Less than 59
A- 90-92	B 83-86	C 73-76	D 63-66	
	B- 80-82	C- 70-72	D- 60-62	

Final Examination Policy

Successful completion of this class requires taking the final examination on its scheduled day. The final examination schedule is posted on the Class Schedules site. If you find yourself scheduled for three (3) or more final examinations on the same day, you are authorized to contact each professor to arrange a different time for one of those exams. However, unless you have three (3) or more exams on the same day, no requests for alternative final examinations will be granted.

Incompletes and Late Assignments

All assignments are to be submitted/turned in by when they are due—including assignments posted in Canvas. Late assignments are deducted 20% of its grade. Incompletes will only be assigned in extremely unusual circumstances.

Missed Exams

No examination shall be missed without prior consent or a well-documented emergency beyond the student's control. A score of zero will be assigned for an examination that is missed without prior consent or a well-documented emergency beyond the student's control. If a student misses an online test, any attempt to complete it outside of the classroom will be considered an act of academic dishonesty and will nullify the test score as well as disciplinary actions.

Class Enrollment

It is the student's responsibility to maintain his/her class schedule. Should the need arise to drop this course (personal emergencies, poor performance, etc.), the student has the responsibility to follow through (provided the drop date meets the stated calendar deadline established by the university), not the instructor. Simply ceasing to attend this course or failing to follow through to arrange for a change of registration (drop/add) may easily result in a grade of F on the official transcript.

PLNU Attendance and Participation Policy

Regular and punctual attendance at all class sessions is considered essential to optimum academic achievement. Unjustified absences or late attendance (i.e., more than 10 minutes) are penalized with a 1% deduction on the overall grade. If the student is absent for more than 10 percent of class sessions, the faculty member will issue a written warning of de-enrollment. If the absences exceed 20 percent, the student may be de-enrolled without notice until the university withdrawal date or, after that date, receive an "F" grade.

Artificial Intelligence (AI) Policy

You are allowed to use Artificial Intelligence (AI) tools (e.g, ChatGPT, iA Writer, Marmot, Botowski, etc.) in this course. Any work that utilizes AI-based tools must be clearly identified as such, including the

specific tool(s) used. For example, if you use ChatGPT, you must cite ChatGPT including the version number, year, month and day of the query and the statement “Generated using OpenAI. https://chat.openai.com/"

PLNU Copyright Policy

Point Loma Nazarene University, as a non-profit educational institution, is entitled by law to use materials protected by the US Copyright Act for classroom education. Any use of those materials outside the class may violate the law.

PLNU Academic Honesty Policy

Students should demonstrate academic honesty by doing original work and by giving appropriate credit to the ideas of others. Academic dishonesty is the act of presenting information, ideas, and/or concepts as one’s own when in reality they are the results of another person’s creativity and effort. A faculty member who believes a situation involving academic dishonesty has been detected may assign a failing grade for that assignment or examination, or, depending on the seriousness of the offense, for the course. Faculty should follow and students may appeal using the procedure in the university Catalog. See Academic Policies for definitions of kinds of academic dishonesty and for further policy information.

PLNU Academic Accommodations Policy

PLNU is committed to providing equal opportunity for participation in all its programs, services, and activities. Students with disabilities may request course-related accommodations by contacting the Educational Access Center (EAC), located in the Bond Academic Center (EAC@pointloma.edu or 619-849-2486). Once a student’s eligibility for an accommodation has been determined, the EAC will issue an academic accommodation plan (“AP”) to all faculty who teach courses in which the student is enrolled each semester.

PLNU highly recommends that students speak with their professors during the first two weeks of each semester/term about the implementation of their AP in that particular course and/or if they do not wish to utilize some or all of the elements of their AP in that course.

Students who need accommodations for a disability should contact the EAC as early as possible (i.e., ideally before the beginning of the semester) to assure appropriate accommodations can be provided. It is the student’s responsibility to make the first contact with the EAC.

State Authorization

State authorization is a formal determination by a state that Point Loma Nazarene University is approved to conduct activities regulated by that state. In certain states outside California, Point Loma Nazarene University is not authorized to enroll online (distance education) students. If a student moves to another state after admission to the program and/or enrollment in an online course, continuation

within the program and/or course will depend on whether Point Loma Nazarene University is authorized to offer distance education courses in that state. It is the student's responsibility to notify the institution of any change in his or her physical location. Refer to the map on State Authorization to view which states allow online (distance education) outside of California.

Semester Schedule Outline

Session	**Topic**
Session 1	Welcome
Session 2	Basic Concepts
Session 3	Binary Numbers
Session 4	Digital Number Systems
Session 5	Boolean Gates
Session 6	Circuits from Boolean Expressions
Session 7	Boolean Theorems
Session 8	NAND, NOR, and Alternate Representations
Session	Designing Logic Circuits
Session 10	Simplifying Logic Circuits
Session 11	Designing Combinational Logic Circuits
Session 12	Karnaugh Maps
Session 13	XOR, XNOR, and Enable/Disable
Session 14	Latches and Clock Signals
Session 15	Clocked Flip-Flops
Session 16	Data Storage with Flip-Flops
Session 17	Counting with Flip-Flops
Session 18	Binary Arithmetic
Session 19	Adder Circuits
Session 20	Asynchronous Counters
Session 21	Synchronous Counters
Session 22	Counters with Mod Numbers < 2^N
Session 23	Up/Down and Presettable Counters
Session 24	State Machines
Session 25	Digital Systems Projects