POINT 1902 LOMA
NAZARENE UNIVERSITY

Department of Physics and Engineering

EGR3093/L Digital Electronics and Lab

2 Units + 1 Lab Unit

Spring 2026

MW | 8:30 - 9:25 AM ; R | 7:25 AM - 10:15 AM

Meeting location Rohr Science Hall (RS) 365

Final Exam: 05/04 7:30 AM - 10:00 AM

Instructor Title and Name: Dr. José Manjarrés
Phone: (619) 849-2451
Email: josemanjarres@pointloma.edu
Office Location and Office Hours: RS 276 | M 9:30-10:30 AM; T 10:00 AM-12:00 PM; W 1:30-3:00 PM; R 10:30 AM – 12:00 PM; F 9:00-10:30 AM

PLNU Mission

To Teach ~ To Shape ~ To Send

Point Loma Nazarene University exists to provide higher education in a vital Christian community where minds are engaged and challenged, character is modeled and formed, and service is an expression of faith. Being of Wesleyan heritage, we strive to be a learning community where grace is foundational, truth is pursued, and holiness is a way of life.

Department Mission

The Department of Physics & Engineering provides strong programs of study that aid in ensuring our students are well prepared for both graduate studies and careers in a variety of scientific and engineering fields. We emphasize a collaborative learning environment that allows students to thrive academically, build personal confidence, and develop interpersonal skills, while providing a Christian setting for students to learn values and judgment and pursue integration of modern scientific knowledge and Christian faith.

Course Description

Boolean algebra, logic gates, combinational logic circuits, state minimization, flip/flops, sequential circuits, asynchronous and synchronous counters. The course emphasizes design aspects using electronic design software.

Prerequisite(s): EGR 2024 with a grade of C- or higher.

Corequisite(s): EGR 3093L

Program and Course Learning Outcomes

Program Outcomes:

- An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors. (LO2)
- An ability to communicate effectively with a range of audiences. (LO3)

Course Learning Outcomes:

- Comprehend and apply various number systems such as binary, decimal, and hexadecimal, and effectively perform conversions between these systems.
- Develop a strong understanding of Boolean logic and effectively use truth tables for analyzing and designing logic circuits.
- Describe logic circuits algebraically utilizing Boolean theorems and algebraic simplifications.
- Demonstrate the ability to design and analyze combinational logic circuits, including the application of the Karnaugh Map method.
- Understand and design sequential logic circuits, including flip-flops and their applications in frequency division and counting while considering timing constraints and implications.
- Implement and analyze digital arithmetic circuits.
- Design and interpret state machines to implement digital system projects.

Required Texts and Recommended Study Resources

Students are responsible for having the required course textbooks prior to the first day of class.

All supplemental materials posted on this course site (including articles, book excerpts, or other documents) are provided for your personal academic use. These materials may be protected by copyright law and should not be duplicated or distributed without permission of the copyright owner.

- R. Tokheim, P. Hoppe. *Digital Electronics: Principles and Applications,* 9th edition. McGraw-Hill, 2022. ISBN 9781264449682.

- R. Tokheim, P. Hoppe. *Experiments Manual To Accompany Digital Electronics: Principles and Applications*, 9th edition. McGraw-Hill, 2022. ISBN 9781264270828.

Course Credit Hour Information

In the interest of providing sufficient time to accomplish the stated Course Learning Outcomes, this class meets the PLNU credit hour policy for a 2-unit class delivered over 14 weeks. It is anticipated that students will spend a minimum of 37.5 participation hours per credit hour on their coursework. For this course, students will spend an estimated 75 total hours meeting the course learning outcomes. The time estimations are provided in the Canvas modules.

Assessment and Grading

This course will have four ways to assess knowledge and learning, described as follows.

1. Pre-class readings: Short quiz related to a pre-session reading to be completed before the class session.
2. Entry tickets: Handwritten summaries of the topics addressed in the pre-class readings.
3. Project presentations: In-class short presentations with the highlights of a project.
4. Project reports: Technical document describing the design process, summarizing experiments, and analyzing results of a project.
5. Final Project: A comprehensive design problem encompassing several topics from the course. It includes a report and a presentation to the general public during the time designated for the final exam.

The table below outlines the assessment criteria for this course.

Activity	**Points per Activity**	**Quantity**	**Total Points**
Pre-class Readings	10	19	190
Entry Tickets	15	16	240
Project Reports	100	2	200
Project Presentations	50	2	100
Final Project	300	1	300
			1030

Grades will be based on the following:

Sample Standard Grade Scale Based on Percentages

A	B	C	D	F
A [92.5-100]	B+ [87.5-90)	C+ [77.5-80)	D+ [67.5-70)	F [0-60)
A- [90-92.5)	B [82.5-87.5)	C [72.5-77.5)	D [62.5-67.5)	
	B- [80-82.5)	C- [70-72.5)	D- [60-62.5)	

Final Examination Policy

Successful completion of this class requires taking the final examination on its scheduled day. The final examination schedule is posted on the Traditional Undergraduate Records: Final Exam Schedules site. If you find yourself scheduled for three (3) or more final examinations on the same day, you are authorized to contact each professor to arrange a different time for one of those exams. However, unless you have three (3) or more exams on the same day, no requests for alternative final examinations will be granted.

Incompletes and Late Assignments

All assignments are to be submitted/turned in by the beginning of the class session when they are due—including assignments posted in Canvas. Late assignments are deducted 20% of its grade. Incompletes will only be assigned in extremely unusual circumstances.

Class Attendance and Punctuality Policy

Regular and punctual attendance at all class sessions is considered essential to optimum academic achievement. Unjustified absences or late attendance (i.e., more than 10 minutes) are penalized with a 1% deduction on the overall grade.

Artificial Intelligence (AI) Policy

You are allowed to use Artificial Intelligence (AI) tools (e.g., ChatGPT, Gemini Pro 1.5, GrammarlyGo, Perplexity, etc) to generate ideas, but you are not allowed to use AI tools to generate content (text, video, audio, images) that will end up in any work submitted to be graded for this course. If you have any doubts about using AI, please gain permission from the instructor.

PLNU Academic Accommodations Policy

PLNU is committed to providing equal opportunity for participation in all its programs, services, and activities in accordance with the Americans with Disabilities Act (ADA). Students with disabilities may

request course-related accommodations by contacting the Educational Access Center (EAC), located in the Bond Academic Center (EAC@pointloma.edu or 619-849-2533). Once a student's eligibility for an accommodation has been determined, the EAC will work with the student to create an Accommodation Plan (AP) that outlines allowed accommodations. Professors are able to view a student's approved accommodations through Accommodate.

PLNU highly recommends that students speak with their professors during the first two weeks of each semester/term about the implementation of their AP in that particular course. Accommodations are not retroactive so clarifying with the professor at the outset is one of the best ways to promote positive academic outcomes.

Students who need accommodations for a disability should contact the EAC as early as possible (i.e., ideally before the beginning of the semester) to assure appropriate accommodations can be provided. It is the student's responsibility to make the first contact with the EAC. Students cannot assume that because they had accommodations in the past, their eligibility at PLNU is automatic. All determinations at PLNU must go through the EAC process. This is to protect the privacy of students with disabilities who may not want to disclose this information and are not asking for any accommodations.

Additional Course Information

Additional PLNU policies and practices that apply to this course can be found at the following link: https://docs.google.com/document/d/11BgAANLOJ9tjt837d24EZ181ukM2qzHF/edit

LomaBooks Instructions for Students

This course is part of our course material delivery program, **LomaBooks***. The bookstore will provide each student with a convenient package containing all required physical materials; all digitally delivered materials will be integrated into Canvas.*

You should have received an email from the bookstore confirming the list of materials that will be provided for each of your courses and asking you to select how you would like to receive any printed components (in-store pick up or home delivery). If you have not done so already, please confirm your fulfillment preference so the bookstore can prepare your materials.

For more information about **LomaBooks,** *please go: HERE*

Semester Schedule Outline

Date	Session	Topic
12-ene	**0**	Welcome
14-ene	**1**	Introduction to Digital Electronics
15-ene	**L1**	Experiment 1-1
19-ene		MLK Day

21-ene	**2**	Binary Game
22-ene	**L2**	Introduction to Verilog and FPGAs
26-ene	**3**	Basic Logic Gates
28-ene	**4**	Basic TTL Gates
29-ene	**L3**	Experiment 3-8
2-feb	**5**	Combining Logic Gates
4-feb	**6**	Boolean Algebra
5-feb	**L4**	Seven-Segment Display Controller in Verilog
9-feb	**7**	Karnaugh Maps
11-feb	**8**	Simple Interfacing
12-feb	**L5**	Project 1 Start
16-feb	**9**	Project 1 Time
18-feb	**10**	Project 1 Time
19-feb	**L6**	Project 1 Presentations
23-feb	**11**	R-S Flip-Flops
25-feb	**12**	J-K Flip-Flops
26-feb	**L7**	Experiments 7-2 and 7-3
2-mar	**13**	Synchronous Counters
4-mar	**14**	Advanced Synchronous Counters
5-mar	**L8**	Experiment 8-7
9-mar		Spring Break
11-mar		Spring Break
12-mar		Spring Break
16-mar	**15**	Count real events like in Figure 8-26 and display on FPGA
18-mar	**16**	Shift Registers
19-mar	**L9**	Experiment 9-5
23-mar	**17**	Project 2 Start
25-mar	**18**	Project 2 Time
26-mar	**L10**	Project 2 Time
30-mar	**19**	Project 2 Presentations
1-abr	**20**	Adders
2-abr		Easter Break
6-abr		Easter Break
8-abr	**21**	IC Adders
9-abr	**L11**	Experiment 10-4
13-abr	**22**	SRAM
15-abr	**23**	ROM
16-abr	**L12**	Experiment 13-1
20-abr	**24**	Final Project Proposals
22-abr	**25**	Final Project Time

23-abr	**L13**	Final Project Time
27-abr	**26**	Final Project Time
29-abr	**27**	Final Project Time
30-abr	**L14**	Final Project Presentations
4-may		Final