Point Loma Nazarene University
EGR 3093 Digital Electronics (3 units)
EGR 3093L Digital Electronics Lab
Spring 2022

CREDIT AND CONTACT HOURS:

Lecture Tue	4:00-5:50 pm	RS 265
Lab Tues.	5:15-7:00 pm	RS 265

INSTRUCTORs: Dr. Tom Carter, Joey Tuttobene

OFFICE HOURS:
Tuesday 3 – 4 pm; location TBD
Otherwise: by appointment on Zoom

TEXTBOOK: *digital electronics, a practical approach with VHDL, 9th edition*, W Kleitz

REFERENCES/SUPPLEMENTS: *LogiSim, Quartus Lite, EDA Playground, Modelsim*

CATALOG:

EGR3093 Digital Electronics (2)
Boolean algebra, logic gates, combinational logic circuits, state minimization, flip/flops, sequential circuits, asynchronous and synchronous counters. Course emphasizes design aspects using electronic design software.

EGR2024L Electric Circuits Analysis Lab (1)
A lab course designed for a hands-on exploration of Digital Electronics & FPGA design.

COURSE LEARNING OUTCOMES/EXPECTED PERFORMANCE CRITERIA:

PROGRAM OUTCOMES: The objectives of the course are to:

1. Understand the concepts of basic digital electronics and design, the theory of Boolean algebra, logic devices and switching theory.
2. Understand digital logic elements, combinational & sequential circuits, & gate reduction.
3. Learn to design, debug and integrate digital logic circuits
4. Learn to design, debug and integrate digital logic for FPGA implementation using both schematic capture and VHDL programming.
5. Understand and analyze multiplexers, demultiplexers, flip/flop devices, finite state machines, asynchronous and synchronous counters, shift registers and correlators.
6. Study the use of encoders and converters, clocks, timers and practical implementations.
7. Study interfacing with non-digital devices such as Analog to Digital converters, LED displays, LCD crystal displays.
8. Study and analyze memory devices, memory size, organization and allocation, ROM, RAM, and programmable ROM.
9. Become competent in designing and building digital systems with FPGA's and standard interfaces

GRADING

Homework	25%	(lowest score for the semester will be dropped)
Lab (+quizzes & project)	25%	(lowest score for the semester will be dropped)
Midterm #1	15%	
Midterm #2	15%	
Final	20%	

Final grades will be determined as follows:

100-93%	A
90-92.9%	A-
87-89.9%	B+
83-86.9%	B
80-82.9%	B-
77-79.9%	C+
73-76.9%	C
70-72.9%	C-
67-69.9%	D+
63-66.9%	D
60-62.9%	D-
0-59.9%	F

COURSE ORGANIZATION

Lectures: PowerPoint and interactive discussion will cover the topics below. Lectures will be posted on Canvas after the class.

Homework: will be assigned weekly on Tuesdays and due before the end of the day on the following Tuesday (some of homework may be germane to the lab on Thursday). Homework should be submitted on Canvas as either text or attached file (which can include pictures of handwritten work, if clearly legible). If delivered late, but by the end of the next day (Wednesday), the grade will be reduced to a max of 80% of original possible points. No late homework will be accepted after that. The lowest grade of homework assignments for the semester will be dropped.

Lab: will be conducted on Thursday and will provide hands-on experience with discrete component circuits as well as FPGA programming based on designs related to the material being covered at that time. Some of the lab time may also be used for interactive problem sessions or simulation, as needed. Lab results will be documented and turned in via Canvas unless otherwise stated. Much of the lab work will be done individually, however there will be opportunity to collaborate during lab period, so communication may factor into the grade. Many labs will require prior preparation and you may be individually quizzed on your understanding of that material before proceeding with the lab. Quiz results will be part of that lab grade. The lowest lab grade for the semester will be dropped. A final lab project, which will include some design creativity, is planned for the end of the semester and may be spread over multiple lab sessions with each graded on the current expected step in the process.

Midterms: Two midterms will be given, based on the material covered during that period of the class. Your own personal handwritten notes may be used on these exams, along with a dedicated calculator but nothing else unless noted. Phones and computers will not be allowed. Some programming may comprise a portion of the exam.

Final: The Final will be comprehensive, covering the material of the entire semester. Your own personal handwritten notes and a calculator may be used on the Final.

If you will miss a class or exam for a school function, you must arrange to make it up **ahead of time**. It is your responsibility to let the professor know of such an absence enough ahead of time to accommodate. Absences due to unexpected emergencies will require documentation from a reliable and verifiable source of the time and reason for such absence.

UNIVERSITY MISSION

Point Loma Nazarene University exists to provide higher education in a vital Christian community where minds are engaged and challenged, character is modeled and formed, and service is an expression of faith. Being of Wesleyan heritage, we strive to be a learning community where grace is foundational, truth is pursued, and holiness is a way of life.

DEPARTMENT MISSION

The Physics and Engineering Department at PLNU provides strong programs of study in the fields of Physics and Engineering. Our students are well prepared for graduate studies and careers in scientific and engineering fields. We emphasize a collaborative learning environment which allows students to thrive academically, build personal confidence, and develop interpersonal skills. We provide a Christian environment for students to learn values and judgment, and pursue integration of modern scientific knowledge and Christian faith.

STATE AUTHORIZATION

State authorization is a formal determination by a state that Point Loma Nazarene University is approved to conduct activities regulated by that state. In certain states outside California, Point Loma Nazarene University is not authorized to enroll online (distance education) students. If a student moves to another state after admission to the program and/or enrollment in an online course, continuation within the program and/or course will depend on whether Point Loma Nazarene University is authorized to offer distance education courses in that state. It is the student's responsibility to notify the institution of any change in his or her physical location. Refer to the map on State AuthorizationLinks to an external site. to view which states allow online (distance education) outside of California.

INCOMPLETES AND LATE ASSIGNMENTS

All assignments are to be submitted/turned in by the time due —including assignments posted in Canvas. Incompletes will only be assigned in extremely unusual circumstances.

PLNU COPYRIGHT POLICY

Point Loma Nazarene University, as a non-profit educational institution, is entitled by law to use materials protected by the US Copyright Act for classroom education. Any use of those materials outside the class may violate the law.

PLNU ACADEMIC HONESTY POLICY

Students should demonstrate academic honesty by doing original work and by giving appropriate credit to the ideas of others. Academic dishonesty is the act of presenting information, ideas, and/or concepts as one's own when in reality they are the results of another person's creativity and effort. A faculty member who believes a situation involving academic dishonesty has been detected may assign a failing grade for that assignment or examination, or, depending on the seriousness of the offense, for the course. Faculty should follow and students may appeal using the procedure in the university Catalog. See Academic PoliciesLinks to an external site. for definitions of kinds of academic dishonesty and for further policy information.

FINAL EXAM

The final exam date and time is set by the university at the beginning of the semester and may not be changed by the instructor. This schedule can be found on the university website and in th course calendar. No requests for early examinations will be approved. Only in the case that a student is required to take three exams during the same day of finals week, is an instructor authorized to consider changing the exam date and time for that particular student.

PLNU ACADEMIC ACCOMMODATIONS POLICY

PLNU is committed to providing equal opportunity for participation in all its programs, services, and activities. Students with disabilities may request course-related accommodations by contacting the Educational Access Center (EAC), located in the Bond Academic Center (EAC@pointloma.edu or 619-849-2486). Once a student's eligibility for an accommodation has been determined, the EAC will issue an academic accommodation plan ("AP") to all faculty who teach courses in which the student is enrolled each semester.

PLNU highly recommends that students speak with their professors during the first two weeks of each semester/term about the implementation of their AP in that particular course and/or if they do not wish to utilize some or all of the elements of their AP in that course.

Students who need accommodations for a disability should contact the EAC as early as possible (i.e., ideally before the beginning of the semester) to assure appropriate accommodations can be provided. It is the student's responsibility to make the first contact with the EAC.

PLNU ATTENDANCE AND PARTICIPATION POLICY

Attendance (in class or online) is expected at each class session. In the event of an absence you are responsible for the material covered in class and the assignments given that day.

Regular and punctual attendance at all classes is considered essential to optimum academic achievement. If the student is absent from more than 10 percent of class meetings, the faculty member can file a written report which may result in de-enrollment. If the absences exceed 20 percent, the student may be de-enrolled without notice until the university drop date or, after that date, receive the appropriate grade for their work and participation. See Academic PoliciesLinks to an external site. for further information about class attendance.

SPIRITUAL CARE

Please be aware PLNU strives to be a place where you grow as whole persons. To this end, we provide resources for our students to encounter God and grow in their Christian faith. If students have questions, a desire to meet with the chaplain or have prayer requests you can contact the Office of Spiritual Development Links to an external site.

CLASS ENROLLMENT

It is the student's responsibility to maintain his/her class schedule. Should the need arise to drop this course (personal emergencies, poor performance, etc.), the student has the responsibility to follow through (provided the drop date meets the stated calendar deadline established by the university), not the instructor. Simply ceasing to attend this course or failing to follow through to arrange for a change of registration (drop/add) may easily result in a grade of F on the official transcript.

CREDIT HOURS:
In the interest of providing sufficient time to accomplish the stated course learning outcomes, this class meets the PLNU credit hour policy for a 3 unit class and 1 unit lab delivered over 15 weeks. Details about how the class meets the credit hour requirements can be provided upon request.

EXPECTED COURSE SCHEDULE BY Date:

LECTURE	TENTATIVE SCOPE (* not covered entirely in text)	TEXT SECTIONS	LAB	Probable Date
1	Digital vs Analog, Number Systems & Apps	Chapter 1	Intro	1/13
2	Digital Electronic Signals/Switches*, Logic Gates	Chapter 2 & 3		1/18
			Logisim	1/20
3	More Logic Gates & Boolean Algebra *	6.1-6.2, 5.1-5.7		1/25
			AND/OR	1/27
4	Boolean Reduction Techniques & Timing *, PLD	5.8-.10, 4.1-.5		2/1

			XOR/XNOR	2/3
5	HDL, VHDL & ModelSim *	6.3-6.5		2/8
			Quartus/VHDL	2/10
6	Binary Arithmetic & Midterm review			2/15
	1st MIDTERM EXAM (lab period)			2/17
7	Arithmetic Circuits* & Mux/Demux, Decoders*	7.1-7.11, 8		2/22
			VHDL Demuxing	2/24
8	Flip-Flops & Registers*, Synchronous Design	10 & 11		3/1
			VHDL Comparator	3/3
	SPRING BREAK	no class		3/8
		no class		3/10
9	Synchronous Design & Finite State Machines *	Chapter 12		3/15
			VHDL Traffic FSM	3/17
10	Counters, Shift Registers & Correlators *	Chapter 13		3/22
			VHDL Max Linear-Feedback Shift Register	3/24
11	Catch Up/Midterm Review/ Final Project			4/7
	2nd MIDTERM EXAM	no lab		3/26
12	Clocks & Timers, Memory & Interfacing *	14, 16.1-16.5		3/29
			VHDL Correlator & Counter Circuits	3/31
13	Industry speakers			4/5
			Final Project work	4/7
14	Design Process, Catch Up	Chapter 15		4/12
			Final Project work	4/14
15	Industry speakers			4/19
			Final Project Presentations	4/21
16	Catch Up/Review for Final			4/26
			Final Project Presentations	4/28